

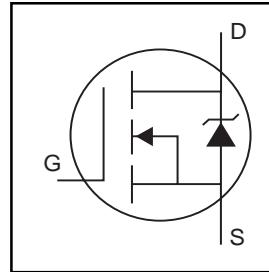
HEXFET® Power MOSFET

- Logic-Level Gate Drive
- Advanced Process Technology
- Ultra Low On-Resistance
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated

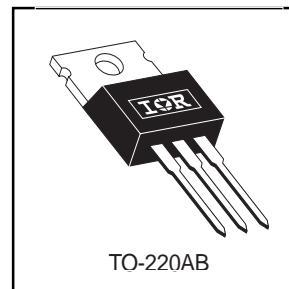
Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve the lowest possible on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The TO-220 package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 watts. The low thermal resistance and low package cost of the TO-220 contribute to its wide acceptance throughout the industry.



$V_{DSS} = 40V$
$R_{DS(on)} = 0.0065\Omega$
$I_D = 130A^{\circledcirc}$



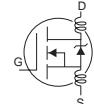
Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	130 ^⑤	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	92 ^⑤	
I_{DM}	Pulsed Drain Current ①	520	
$P_D @ T_C = 25^\circ C$	Power Dissipation	200	W
	Linear Derating Factor	1.3	W/ $^\circ C$
V_{GS}	Gate-to-Source Voltage	± 16	V
E_{AS}	Single Pulse Avalanche Energy ②	700	mJ
I_{AR}	Avalanche Current ①	78	A
E_{AR}	Repetitive Avalanche Energy ①	20	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.0	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	$^\circ C$
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torque, 6-32 or M3 screw	10 lbf·in (1.1N·m)	

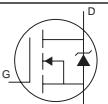
Thermal Resistance

	Parameter	Typ.	Max.	Units
R_{qJC}	Junction-to-Case	—	0.75	$^\circ C/W$
R_{qCS}	Case-to-Sink, Flat, Greased Surface	0.50	—	
R_{qJA}	Junction-to-Ambient—	62	—	

Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(\text{BR})\text{DSS}}$	Drain-to-Source Breakdown Voltage	40	—	—	V	$V_{GS} = 0V, I_D = 250\mu\text{A}$
$\Delta V_{(\text{BR})\text{DSS}}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.04	—	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D = 1\text{mA}$
$R_{DS(\text{on})}$	Static Drain-to-Source On-Resistance	—	—	0.0065	W	$V_{GS} = 10V, I_D = 78\text{A}$ ④
		—	—	0.009		$V_{GS} = 4.5V, I_D = 65\text{A}$ ④
$V_{GS(\text{th})}$	Gate Threshold Voltage	1.0	—	—	V	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$
g_{fs}	Forward Transconductance	63	—	—	S	$V_{DS} = 25V, I_D = 78\text{A}$
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	$V_{DS} = 40V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 32V, V_{GS} = 0V, T_J = 150^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 16V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -16V$
Q_g	Total Gate Charge	—	—	100	nC	$I_D = 78\text{A}$
Q_{gs}	Gate-to-Source Charge	—	—	32		$V_{DS} = 32V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	43		$V_{GS} = 4.5V, \text{See Fig. 6 and 13}$ ④
$t_{d(on)}$	Turn-On Delay Time	—	—	16		$V_{DD} = 20V$
t_r	Rise Time	—	—	210	ns	$I_D = 78\text{A}$
$t_{d(off)}$	Turn-Off Delay Time	—	—	25		$R_G = 2.5\text{W}, V_{GS} = 4.5V$
t_f	Fall Time	—	—	14		$R_D = 0.18\text{W}, \text{See Fig. 10}$ ④
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	—	7.5	—		
C_{iss}	Input Capacitance	—	5330	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	1480	—		$V_{DS} = 25V$
C_{rss}	Reverse Transfer Capacitance	—	320	—		$f = 1.0\text{MHz}, \text{See Fig. 5}$

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	130⑤	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	520		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 78\text{A}, V_{GS} = 0V$ ④
t_{rr}	Reverse Recovery Time	—	78	120	ns	$T_J = 25^\circ\text{C}, I_F = 78\text{A}$
Q_{rr}	Reverse Recovery Charge	—	180	270	nC	$dI/dt = 100\text{A}/\mu\text{s}$ ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- ② Starting $T_J = 25^\circ\text{C}$, $L = 0.23\text{mH}$
 $R_G = 25\text{W}, I_{AS} = 78\text{A}$. (See Figure 12)
- ③ $I_{SD} \leq 78\text{A}$, $di/dt \leq 370\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(\text{BR})\text{DSS}}$, $T_J \leq 175^\circ\text{C}$

④ Pulse width $\leq 300\mu\text{s}$; duty cycle $\leq 2\%$

⑤ Calculated continuous current based on maximum allowable junction temperature; for recommended current-handling of the package refer to Design Tip #93-4

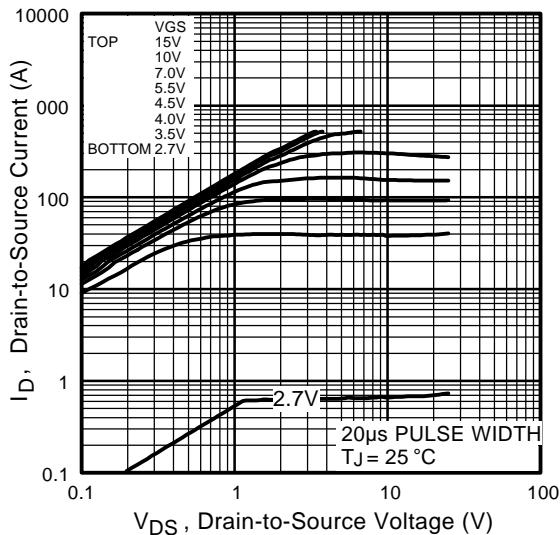


Fig 1. Typical Output Characteristics

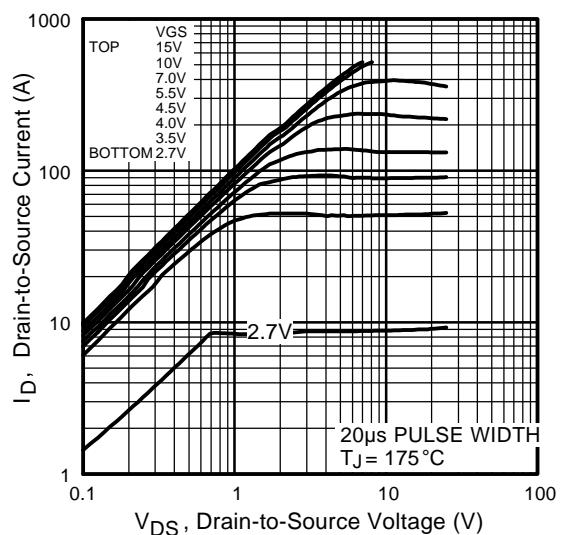


Fig 2. Typical Output Characteristics

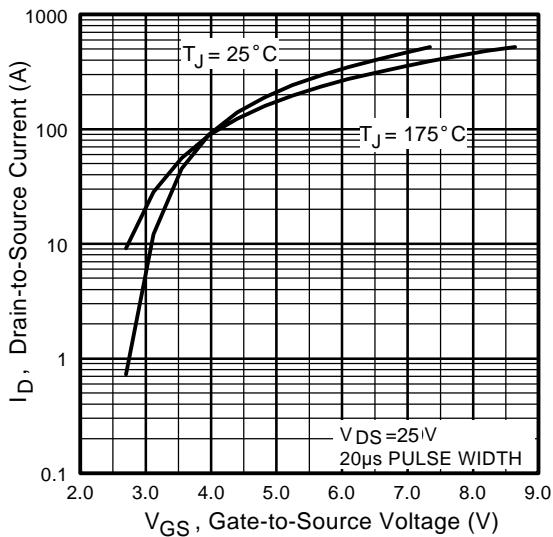


Fig 3. Typical Transfer Characteristics

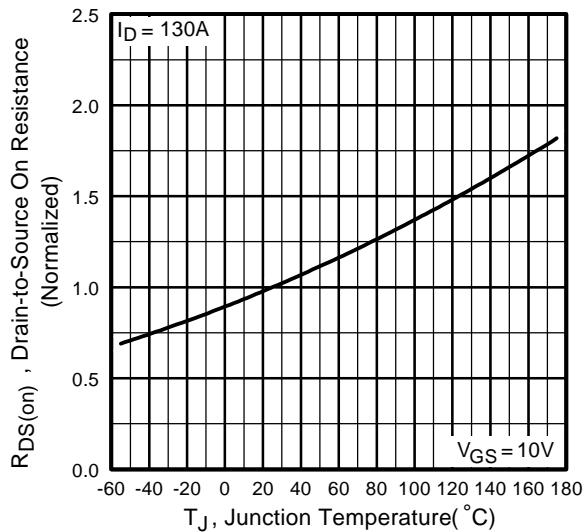


Fig 4. Normalized On-Resistance Vs. Temperature

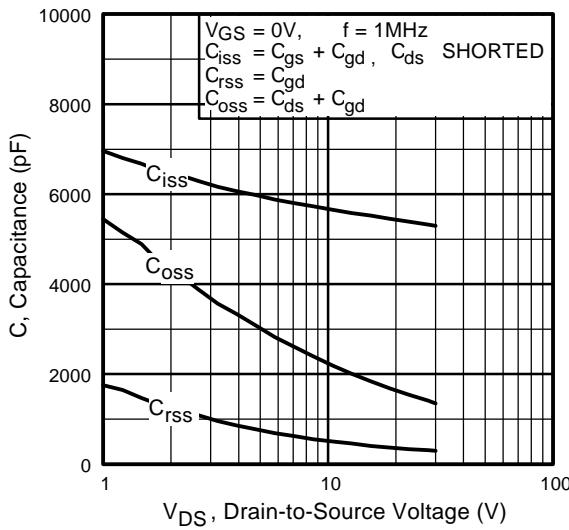


Fig 5. Typical Capacitance Vs.
Drain-to-Source Voltage

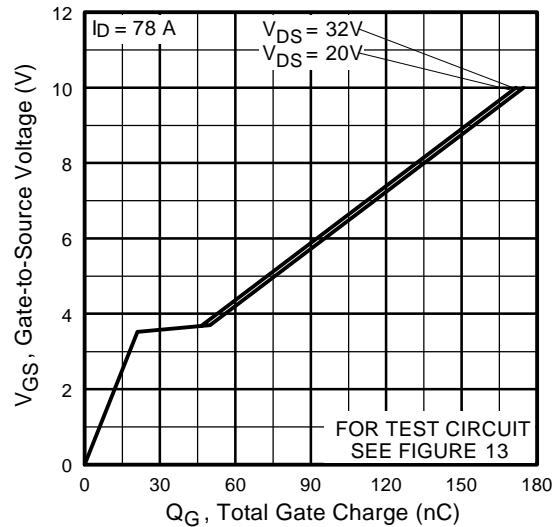


Fig 6. Typical Gate Charge Vs.
Gate-to-Source Voltage

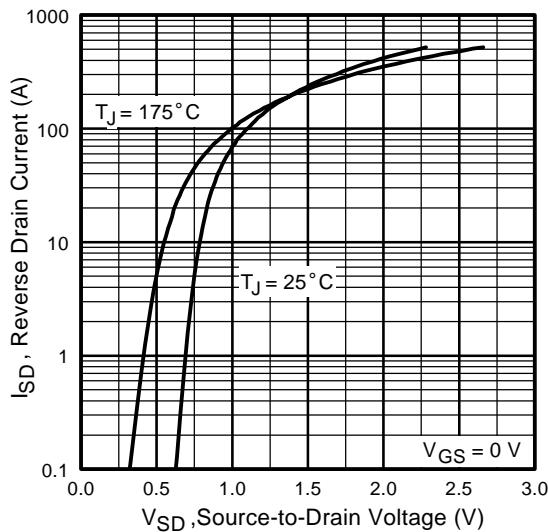


Fig 7. Typical Source-Drain Diode
Forward Voltage

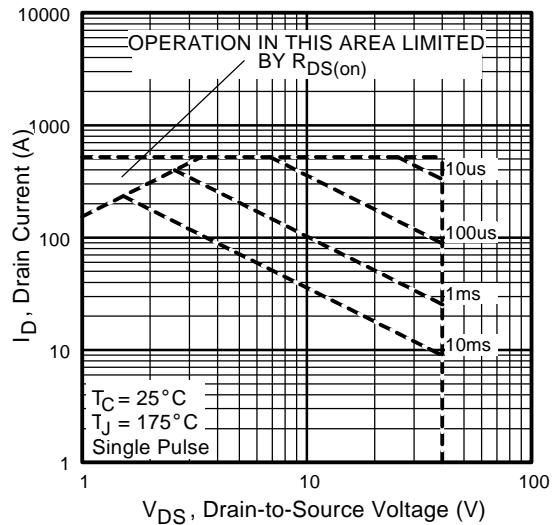


Fig 8. Maximum Safe Operating Area

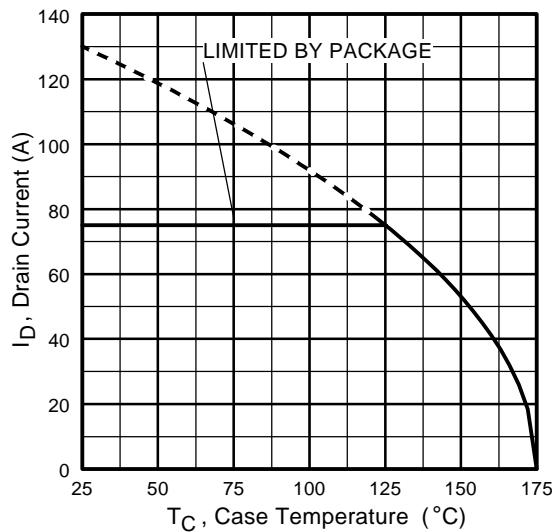


Fig 9. Maximum Drain Current Vs.
Case Temperature

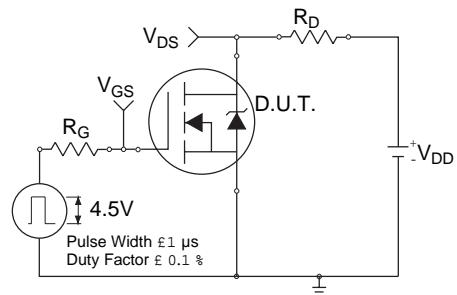


Fig 10a. Switching Time Test Circuit

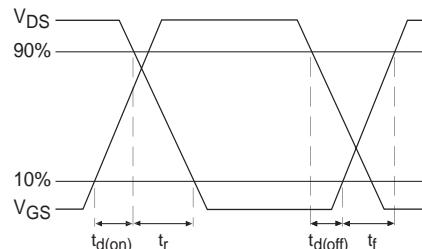


Fig 10b. Switching Time Waveforms

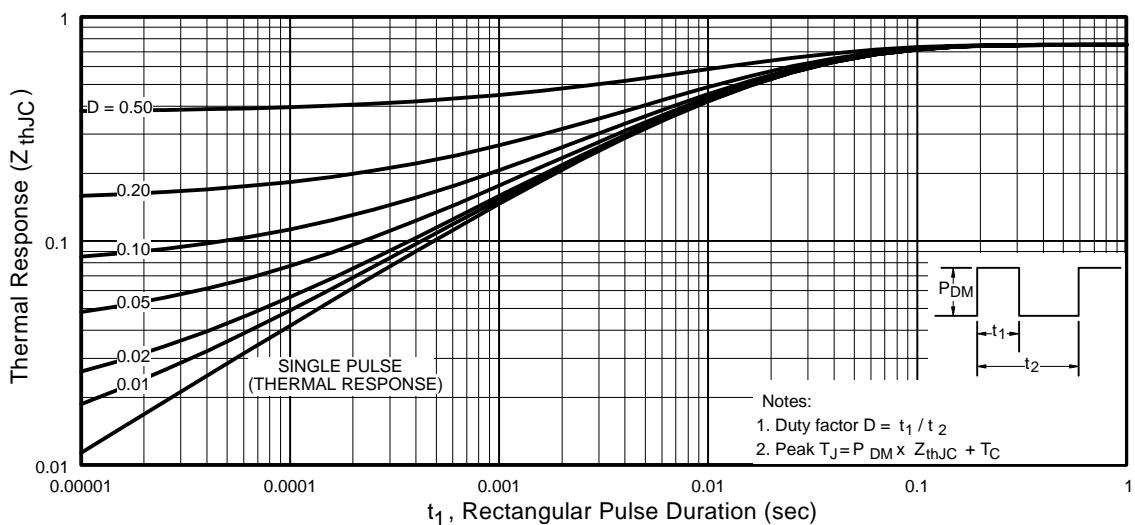
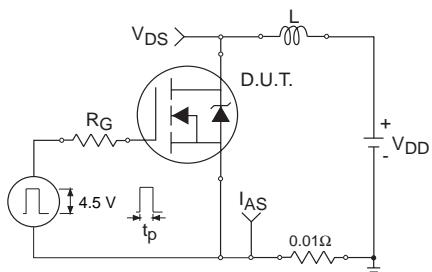
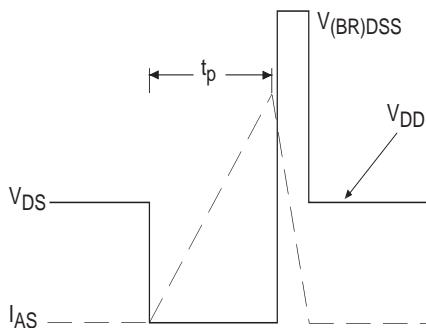
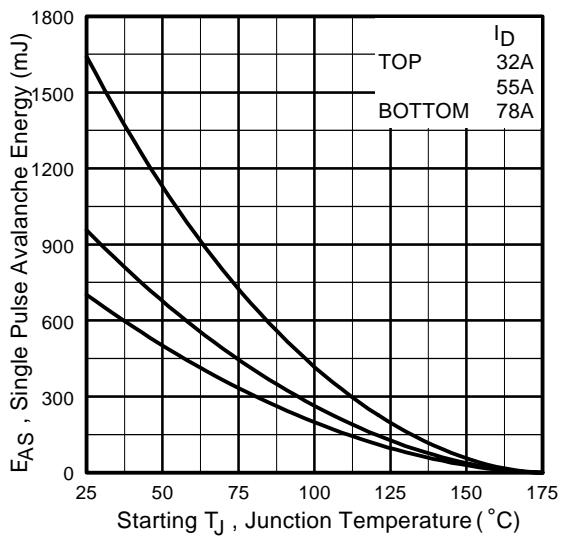
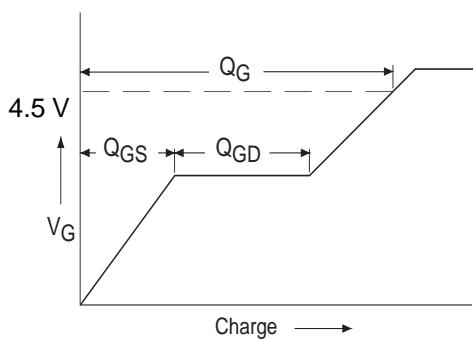
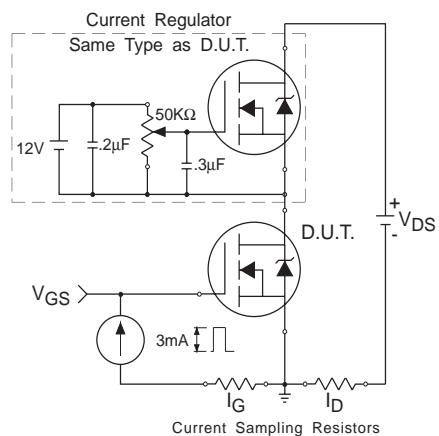
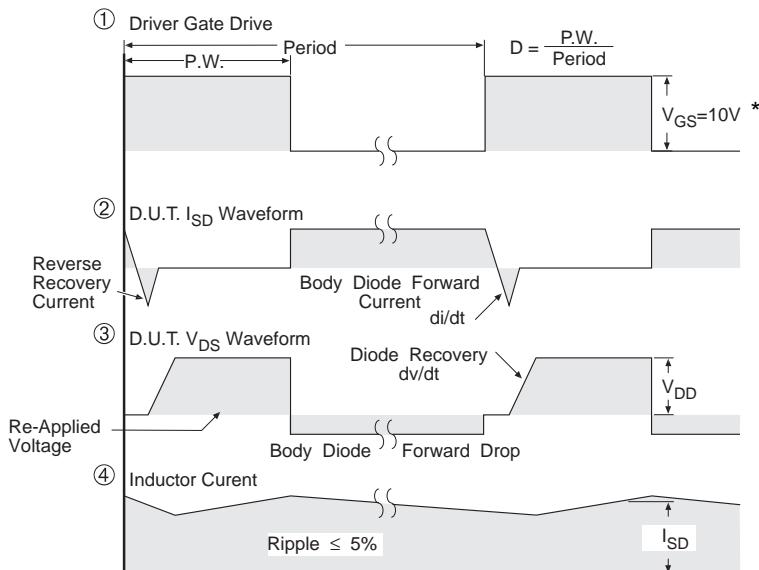
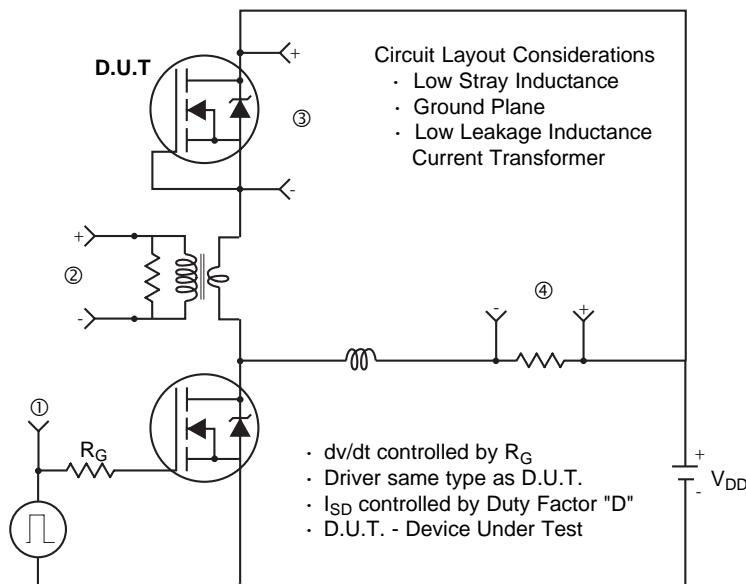


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

**Fig 12a.** Unclamped Inductive Test Circuit**Fig 12b.** Unclamped Inductive Waveforms**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current**Fig 13a.** Basic Gate Charge Waveform**Fig 13b.** Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



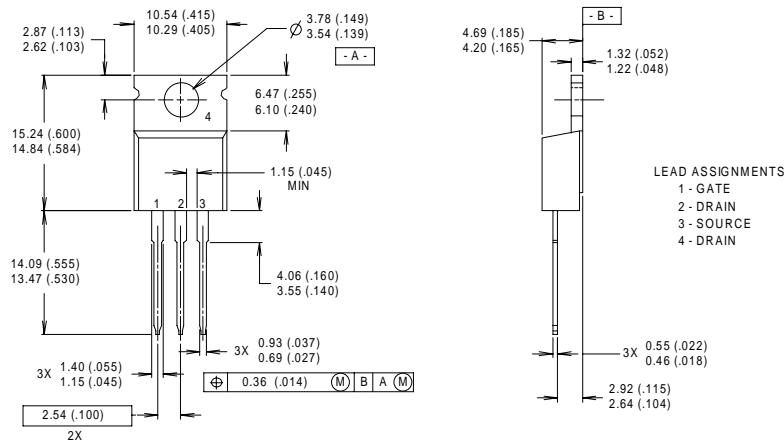
* $V_{GS} = 5V$ for Logic Level Devices

Fig 14. For N-Channel HEXFETS

Package Outline

TO-220AB Outline

Dimensions are shown in millimeters (inches)



NOTES:

1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.

2 CONTROLLING DIMENSION : INCH

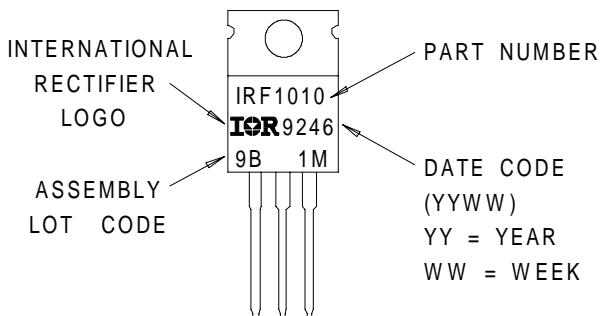
3 OUTLINE CONFORMS TO JEDEC OUTLINE TO-220AB.

4 HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.

Part Marking Information

TO-220AB

EXAMPLE : THIS IS AN IRF1010
WITH ASSEMBLY
LOT CODE 9B1M



International
IR Rectifier

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IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 6172 96590

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